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Stoye, W. Greaves, D. Richards, N. Green, J. Tension Technology EDA;

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translating verilog to c++

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A Ghosh, J Kunkel, S Liao - Proceedings of the conference on Design, automation and test ..., 1999 - portal.acm.org

... **translation** time, but eliminates bugs during **translation** which can ... sub-tying and

virtual function facilities of C++. ... similar to always blocks in **Verilog** or a ...

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G De Micheli - Design, Automation and Test in Europe Conference and ..., 1999 - ieeexplore.ieee.org

... circuits and systems using C/C++, perform functional sim- ulation, and then **translate**

the portion ... description language (HDL), such as **Verilog** HDL or ...

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[A C++ ASIC Design Methodology Facilitated by a C++-Verilog Translator](#)

D Joyce, A Nowatzky, R Stets - 10th International HDL Conference, 2001 - research.compaq.com

... We decided to investigate tools for C++ to **Verilog translation**. In ... The L1

C++ code was then ready for **translation** to **Verilog**. For ...

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[A survey of techniques used in the synthesis of hardware from C/C++ as a part of hardware/software ...](#)

K Ramani, RL Haggard - Southeastern Symposium on System Theory,

2001. Proceedings ..., 2001 - ieeexplore.ieee.org

... The second method to synthesize the C/C++ into hardware is to **translate** a subset of C into an HDL (VHDL or **Verilog**) that will eventually be synthesized by ...

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[Using C-to-C++ translation for large soc concurrent engineering: a case study - group of 2 »](#)

W Stoye, D Greaves, N Richards, J Green, TT EDA - Electronics Systems and Software, 2003 - ieeexplore.ieee.org

... This work has produced a simple **translation** tool for converting **Verilog** into C with a number of desirable ... VTOC converts synthesisable **Verilog** into C++ ...

[Web Search](#)

[Networked object oriented verification with C++ and Verilog - group of 4 »](#)

G Dearth, S Meeth, P Whittemore - **Verilog** HDL Conference and VHDL International Users Forum, ..., 1998 - doi.ieeeecs.org

... Module (C/C++) ... The stub is responsible for ensuring logical signal propagation throughout the **Verilog** processes. Address **Translation** Interface (ATI) ...

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[Designers May Find C++ to Their Liking - group of 4 »](#)

M Saito - INTEGRATED SYSTEM DESIGN, 2001 - eedesign.com

... convert the C or C++ description to **Verilog** or VHDL ... Or they do not convert the C/C++ model, but ... multiple system tests to verify that the **translation** is accurate ...

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[Methodology for hardware/software co-verification in C/C++\(short paper\) - group of 2 »](#)

L Séméria, A Ghosh - Proceedings of the 2000 conference on Asia South Pacific ..., 2000 - portal.acm.org

... as the co-simulation of C and **Verilog** HDL or ... In a C/C++-based methodology, designer productivity can ... significantly because one can eliminate **translation** from a ...

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The case for C/C++ hardware design - group of 2 »

R Allen, D Gajski - EEDesign, June, 2000 - eedesign.com

... is dominated by the use of **Verilog** and VHDL ... **C++** extends the basic computational facilities in C to ... Technically, **translating** C directly into silicon is not a ...

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System and method for system level and circuit level modeling and design simulation using C++ - group of 3 »

S Li, S Tjiang, R Gupta - US Patent 6,152,612, 2000 - Google Patents

... 135 C++ Library: Timing Constructs Thread / Co-Routine Library

I270200... 720 FIG.

1 1A /* **translation** to char */ const char stdjjlogic: :to_char_table [Ns1] = ...

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